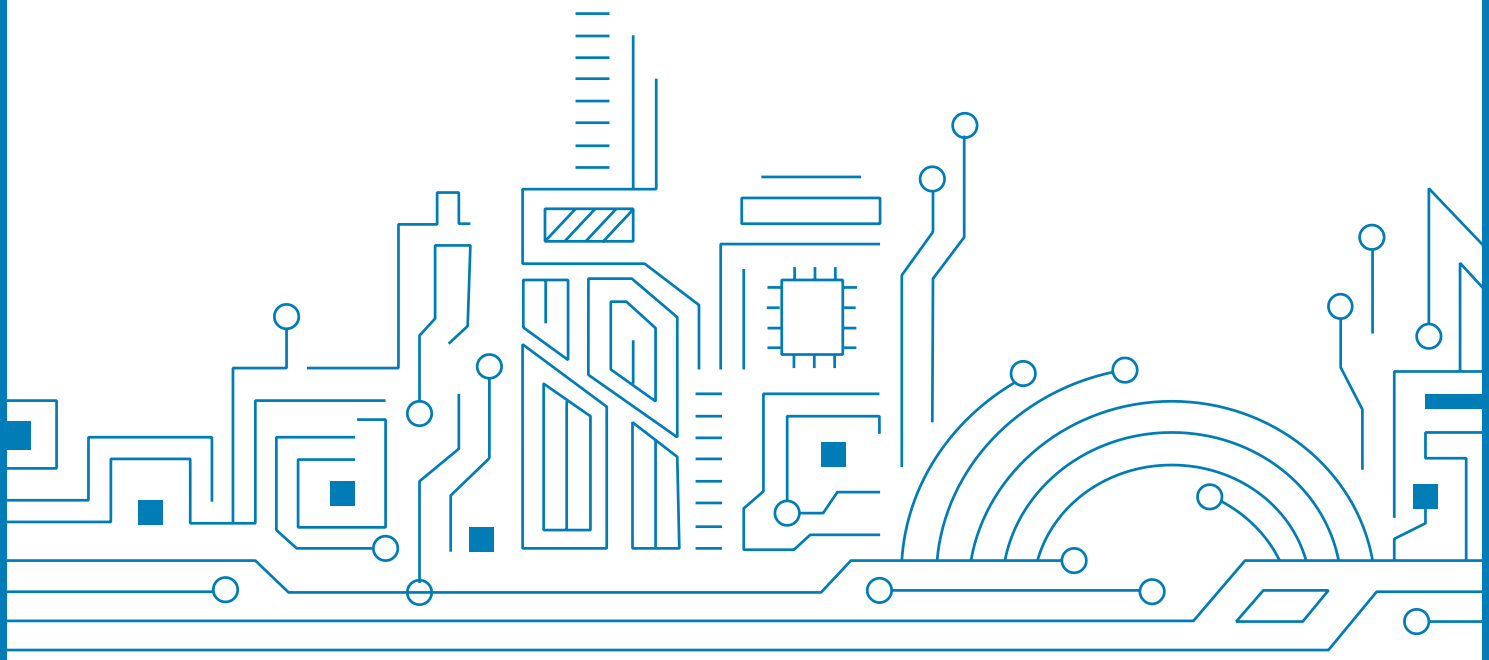
GNSS Dual-band Positioning Module

TAU824M-N200

Datasheet V1.0



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About the Document

Basic info

Document applies to	TAU824M-N200
Document type	Datasheet
Revision and date	V1.0/2026-03
Product status	Mass production

Product status description

In development	Objective specification. Revision may be released in later status.
Engineering sample	Product specifications tested on early. Revision may be released in later status.
Preliminary	Product specifications come from small production. Revision may be released in later status.
Mass production	Final product specification to mass market.

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1 SYSTEM OVERVIEW

1.1 Overview

The TAU824M-N200 is a GNSS dual-band high-precision navigation and positioning module, which is based on the state of art CYNOSURE IV-E GNSS SoC chip. It is capable of tracking all global civil navigation systems (BDS, GPS, GLONASS, Galileo, QZSS, NavIC, and SBAS) in L1 and L5 bands, as well as BDS-3 signals. The newly designed Cynosure architecture makes the module achieve higher sensitivity, greater for improved jam resistance and multipath, and provides a highly robust service in complicated environment.

Integrating an efficient power management unit, this module provides a high-performance and flexible solutions for GNSS navigation applications such as vehicle monitoring and navigation.

1.2 Product Photo



Figure 1 Product diagram

1.3 Features

- Concurrent reception of multi-band multi-system satellite signals
- Tracking L1 and L5 bands signals at the same time
- Support GNSS multi-system and single system positioning
- Support BDS-3 system signals
- Support A-GNSS
- Configure NavIC system positioning only

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Table 1 TAU824M-N200

Product	GNSS						Feature							Interface			Accuracy			Grade	
	Bands (S/D/T)	BDS	GPS/QZSS	GLONASS	Galileo	NavIC	Programmable (Flash)	Built-in SAW	Built-in LNA	Data logging	D-GNSS	Oscillator	Built-in inductor	PPS	UART	I2C	Meter	Sub-meter	Centimeter	Industrial	Automotive
TAU824M-N200	D	●	●	●	●	○	●	●	●	●	●	T	●	●	●	○		●		●	

T = TCXO

○ = Supported upon request with special firmware

1.4 Block diagram

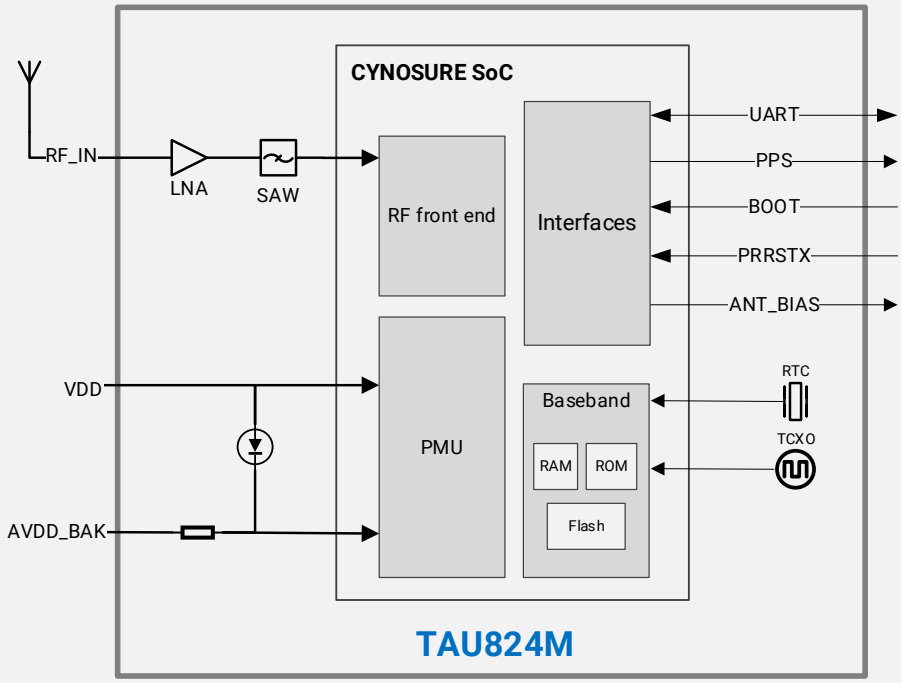


Figure 2 Block diagram

1.5 Specifications

Table 2 Specifications

Parameter	Specification
GNSS channels	160 in total (64 tracking channels)
GNSS reception	GPS/QZSS: L1C/A, L5

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	BDS: B1I, B1C, B2a	
	GLONASS: G1	
	Galileo: E1, E5a	
	NavIC[1]: L5	
	SBAS[1]: L1	
Update rate	1 Hz, by default	
Position accuracy[2]	GNSS	1.0m CEP
	D-GNSS	< 1.0m CEP
Velocity & Time accuracy	GNSS	0.05 m/s CEP
	1PPS	20 ns RMS
TTFF	Hot start	2s
	Cold start	28s
Sensitivity[3]	Cold start	-148 dBm
	Hot start	-156 dBm
	Reacquisition	-156 dBm
	Tracking & navigation	-165 dBm
Protocol	NMEA 0183 Ver. 4.10/4.11 Cynosure GNSS receiver protocol	
Operating condition	Main supply	3.0V to 3.6V
	Digital I/O supply	3.0V to 3.6V
	Backup supply	1.8V to 3.6V
Power consumption	Tracking	41 mA @ 3.3V
	Acquisition	44 mA @ 3.3V
	Standby	13 uA
Serial interface	UART[3]	2
	I2C[3]	1
Operating limit	Velocity	515 m/s
	Altitude	18,000m
Environmental conditions	Operating temperature	-40°C to +85°C
	Storage temperature	-40°C to +90°C
Dimension	16.0×12.2×2.4 mm 24PIN LCC	
Certification	RoHS & REACH	

* *[1] Supported upon request with special firmware.*
* *[2] Open sky, dual-band positioning. Demonstrated with a good external LNA. Different bands show slight deviation.*
* *[3] UART1 and I2C are configured upon request with special firmware.*

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2 PIN DESCRIPTION

2.1 Pin Assignment

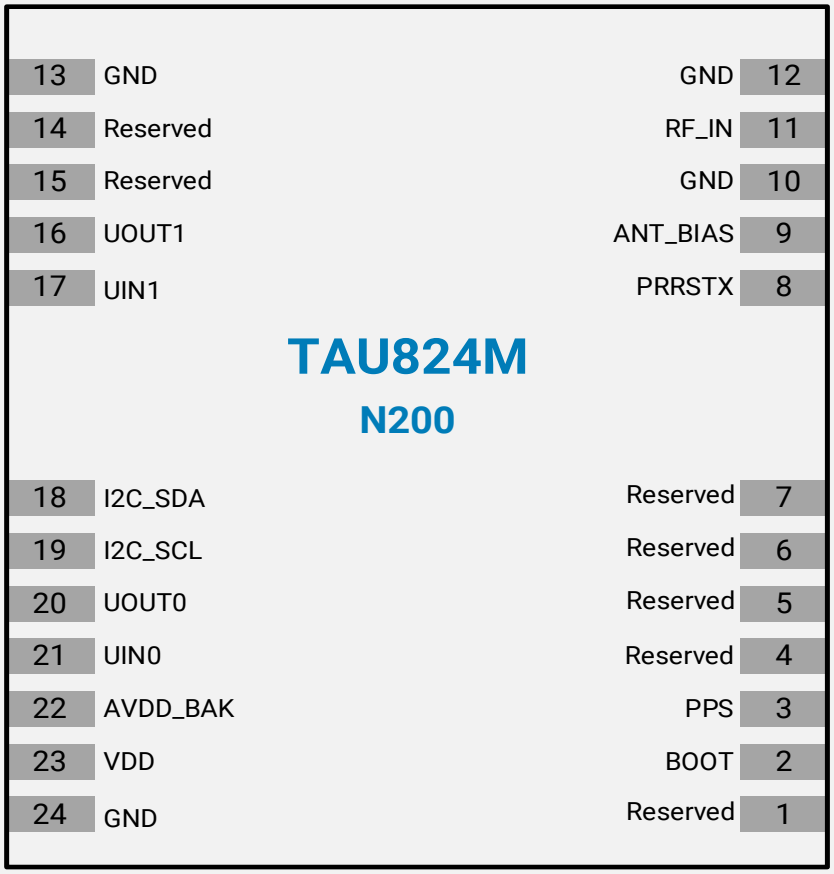


Figure 3 Pin assignment (top view)

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2.2 Detailed pin descriptions

Table 3 Detailed pin descriptions

Function	Symbol	No.	I/O	Description
Power	VDD	23	P	Main supply input: DC 3.3V±10%
	GND	10, 12, 13, 24	VSS	Ground
	AVDD_BAK	22	P	Backup supply input: 1.8V ~ 3.6V
Antenna	RF_IN	11	I	RF section output voltage (50Ω impedance). Used to power the external active antenna. Leave it floating if not used.
	ANT_BIAS	9	O	RF signal input (not greater than 35 mA)
UART	UOUT0	20	O	UART0 serial data output. Leave it floating if not used.
	UIN0	21	I	UART0 serial data input. Leave it floating if not used.
	UOUT1[1]	16	O	UART1 serial data output. Leave it floating if not used.
	UIN1[1]	17	I	UART1 serial data input. Leave it floating if not used.
I2C[1]	I2C_SDA	18	I/O	I^2C data. Leave it floating if not used.
	I2C_SCL	19	I/O	I^2C clock. Leave it floating if not used.
Others	BOOT	2	I	Mode entry. Leave it floating if not used.
	PRRSTX	8	I	External reset, low active. Connect PRRSTX to the MCU during design.
	PPS	3	O	Time pulse output (PPS). Leave it floating if not used.
	Reserved	1, 4, 5, 6, 7, 14, 15	--	Reserved pin. Leave it floating.

* *[1] Supported upon request with special firmware*

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3 ELECTRICAL CHARACTERISTICS

3.1 Absolute Maximum Rating

Table 4 Absolute rating

Symbol	Parameter	Min.	Max.	Unit
VDD	Power input for the main power domain	-0.5	3.63	V
AVDD_BAK	Power input for the backup power domain	-0.5	3.63	V
VI_{max}	Voltage input of I/O pin	-0.5	3.63	V
T_{env}	Operation temperature	-40	85	°C
$T_{storage}$	Storage temperature	-40	90	°C
T_{solder}	Solder reflow temperature	--	260	°C

3.2 IO Characteristics

3.2.1 PRRSTX

Table 5 PRRSTX

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_{IZ}	Input leakage current	--	--	--	+/-1	uA
V_{IH}	Input high voltage	--	AVDD_BAK×0.7	--	AVDD_BAK	V
V_{IL}	Input low voltage	--	0	--	AVDD_BAK×0.3	V

3.2.2 Others

Table 6 Others

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_{IZ}	Input leakage current	--	--	--	+/-1	uA
V_{IH}	Input high voltage	--	VDD×0.7	--	VDD	V
V_{IL}	Input low voltage	--	0	--	VDD×0.3	V
V_{OH}	Output high voltage	I_{OH} = 11.9mA, VDD = 3.3V	2.64	--	--	V
V_{IH}	Input high voltage	I_{OL} = 7.9mA, VDD = 3.3V	--	--	0.4	V

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3.3 DC Characteristics

Table 7 DC Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD	Power input for the main power domain	3.0	3.3	3.6	V
AVDD_BAK	Power input for the backup power domain	1.8	3.3	3.6	V
I_{ANT_BIAS}	ANT_BIAS output current	--	--	35	mA
V_{ANT_BIAS}	ANT_BIAS output voltage	--	VDD-0.2	--	V
ICC_{max}	Maximum operating current @ VDD	--	--	200	mA

3.4 Power Consumption

Table 8 Power consumption

Symbol	Mode	Condition	Typ.	Unit
I_{CCRX1}	Acquisition (GNSS, L1+L5)	VDD[1]	44	mA
I_{CCRX2}	Tracking (GNSS, L1+L5)	VDD[1]	41	mA
I_{CCDBM}	Standby mode	AVDD_BAK[2]	13	uA

* *[1] Condition: VDD = 3.3V. Room temperature. All pins floating.*
* *[2] Condition: AVDD_BAK = 3.3V. Room temperature. All pins floating.*

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4 HARDWARE DESCRIPTION

4.1 Connecting Power

The module has two power supply pins: VDD and AVDD_BAK. The main power is supplied through the VDD pin, and the backup power is supplied through the AVDD_BAK pin. to ensure optimal positioning performance, please minimize the ripple of the module power supply as much as possible. It is recommended to use the LDO of a current above 200 mA.

If the power for VDD pin is off, the real-time clock (RTC) and battery backed RAM (BBR) are supplied through the AVDD_BAK pin. Thus, orbit information and time can be maintained and will allow a Hot or Warm start. If no backup battery is connected, the module will perform a cold start at every power-up if no aiding data is sent to the module.

Note: If no backup supply is available, connect the AVDD_BAK pin to VDD.

4.2 Power on/off Sequence

4.2.1 Initial system power on

Permanent damage may occur with an inappropriate power-on sequence. So, please follow the rules below during design. To meet the requirement of controlling the power on/off sequence of the module, please connect the external reset pin (PRRSTX) to the MCU.

When the VDD powers on from off state, the external reset (PRRSTX) must be active and hold for more than 10 ms before and after the main supply reaches the minimum operating voltage. The system power on sequence is illustrated in Figure 4 System power on sequence .

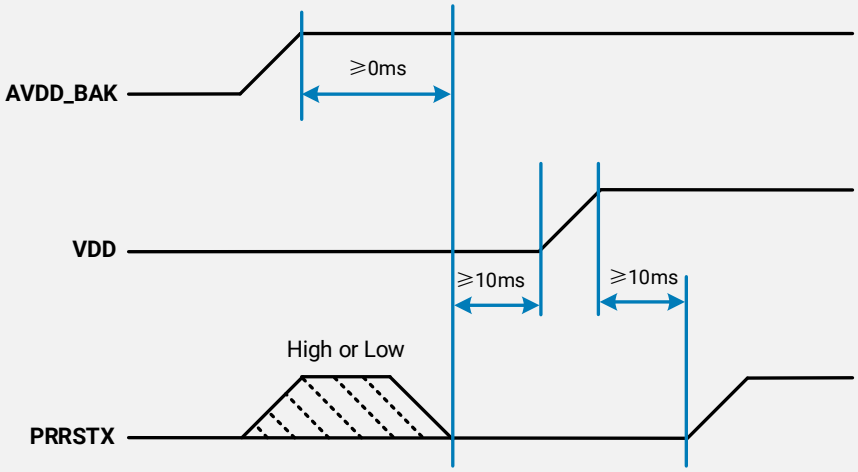


Figure 4 System power on sequence

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4.2.2 Hot start power on

The AVDD_BAK remains on to keep backup data when the VDD is off, and the system remains operational. In this case, keep the PRRSTX at a low level for at least 10 ms before and after the VDD returns to the operating voltage. During this time, the PRRSTX remains at a low level for more than 100 ms. Or, the hot start will fail. Also, after the VDD is off, the supply voltage shall be less than 0.3V.

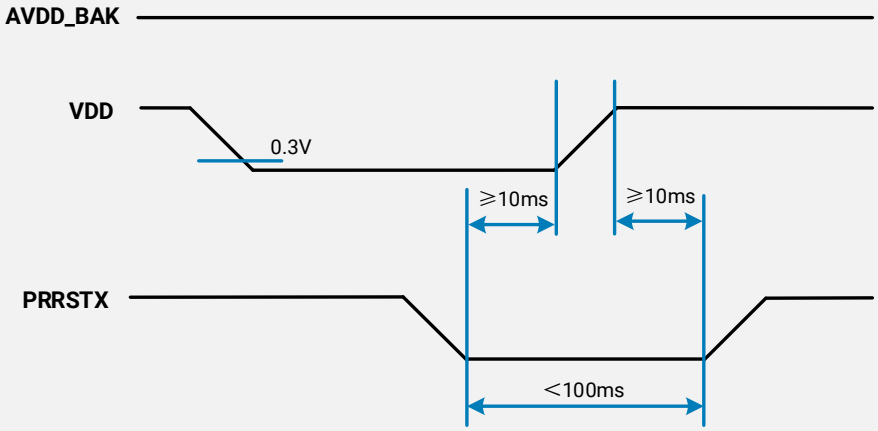


Figure 5 Hot start power on sequence

4.2.3 Power off in the application

Perform the following steps to power off the module:

1) Run the power down command: F1 D9 06 41 05 00 00 00 00 00 03 4F 64

2) Power off the module after 500 ms. Please ensure that the voltage of the main power supply (VDD), backup power supply (AVDD_BAK) (if powered off), and I/O power is below 0.3V, to avoid the residual voltage from affecting the next power-on.

- To wake up the module after sending the power-down command, it is necessary to pull PRRSTX low or disconnect the standby power supply and power it on again.
- The electrical characteristics of each EVK board vary, as does the capacitance and load, which leads to differences in power-off time. Please confirm the power-off time of each EVK with Allystar technical support.

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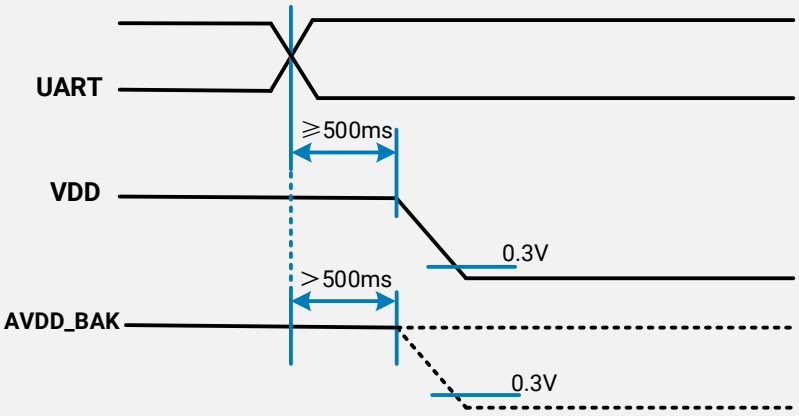


Figure 6 Power off sequence

4.3 Reset and Mode Control

The operation mode is controlled by PRRSTX and BOOT pins. PRRSTX is the reset control pin and BOOT is used for the system upgrade, both of which are active at a low level. An I/O pin with an OD output function or a triode control (pulse width ≥100ms) is recommended.

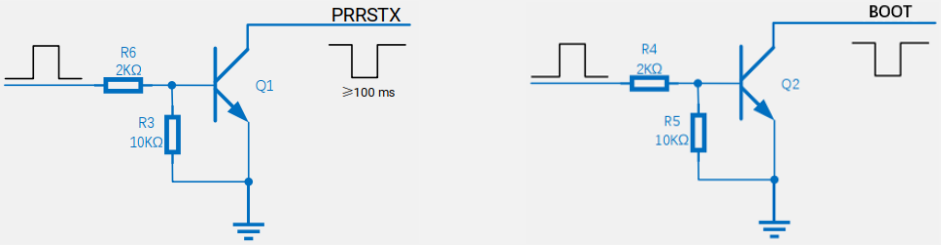


Figure 7 Reset and mode entry

Parameter	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Reset Timing	t_{RSTL}	PRRSTX	Connected to a stable power source, and TCXO clock remains stable.	100	--	--	mS



Figure 8 Reset Timing

While the module works in operation mode, keep PRRSTX and BOOT pins at a high level. The module will enter reset state when PRRSTX being low level (see Figure 9 Mode entry sequence). Operate BOOT and PRRSTX pins as the following instructions to enter **BootROM Command Mode** to update firmware.

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- BOOT trigger: Operate the BOOT and PRRSTX pins at the same time. After entering BootROM mode, the firmware is downloaded via UART to start the upgrade. Once completed, operate the PRRSTX pin to return to User mode.
- User2Boot command: After the system has booted and stabilized the oscillator, send the User2Boot command (F1 D9 06 5F 00 00 65 35) to the module via the UIN0 pin. The hardware circuit will respond during the validity period of the command (about 20 ms when TCXO = 26 MHz). When detecting the command, the system will restart automatically and enter BootROM mode to download the firmware and start to upgrade.

When connecting the PRRSTX and BOOT to any MCU I/O, it is recommended to adopt the I/O pin with the OD output function, DO NOT use the pull-up or pull-down resistance.

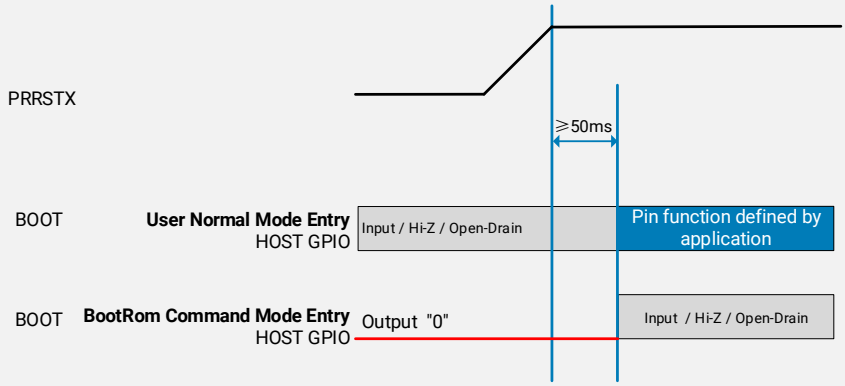


Figure 9 Mode entry sequence

4.4 Antenna Design

There is a built-in LNA and SAW in the module. It is recommended to use an active antenna with a gain less than 30 dB and a noise figure of less than 1.5 dB.

4.4.1 ANT_BIAS

The ANT_BIAS pin powers an external active antenna, see the Reference Design for details. It also provides current detection for real-time monitoring of the antenna status and protection against short circuits.

- **Short circuit protection**
  - » The module provides short circuit detection and protection functions for the antenna. Once an overcurrent is detected at the ANT_BIAS port, the module will restrict current output automatically to protect it from damages.
- **Open circuit detection**
  - » The module can detect an open circuit in the antenna. Users can judge it from antenna status

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messages.

Table 9 Antenna status and NMEA message

Antenna status	Status output	NMEA message
Open circuit	OPEN	$GNTXT,01,01,01,**ANT_OPEN***40
Regular circuit	OK	$GNTXT,01,01,01,**ANT_OK***50
Short circuit	SHORT	$GNTXT,01,01,01,**ANT_SHORT***06

4.5 UART

- Set the UART pin away from ESD devices such as antenna and sensor due to its strong drive capability.
- DO NOT parallel the UART signal with other power or signal lines for a long distance to avoid crosstalk causing interference.

The UART high level may cause a residual voltage on VDD if the UART pin is connected to the MCU normally when the VDD is off, thus resulting in an abnormality when powering on/off. Therefore, when the VDD is off, disconnect the UART, or set the MCU_UART to the input state or high resistance state.

Due to the strong drive capability of the UART pin, installing an RC circuit in a vehicle or other complex application can effectively prevent interference from the UART signal with other signals.

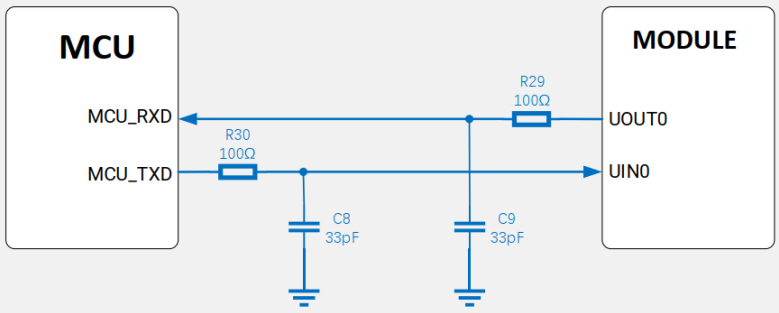


Figure 10 Reference design of UART

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5 DEFAULT MESSAGE

Table 10 Default message

Interface	Settings
UART output	Data format: 1 start bit, 8 data bits, no parity bit, 1 stop bit Default baud: 115200 bps Configured to transmit both NMEA and Allystar's Binary protocols; both NMEA and HD Binary messages are supported.
UART input	Data format: 1 start bit, 8 data bits, no parity bit, 1 stop bit Default baud: 115200 bps Default protocol: Allystar's Binary protocol, NMEA message
PPS	1 pulse per second, synchronized at rising edge, pulse length 100 ms (subject to the firmware configuration)

* *Refer to GNSS_Protocol_Specification for information about other settings.*

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6 MECHANICAL SPECIFICATION

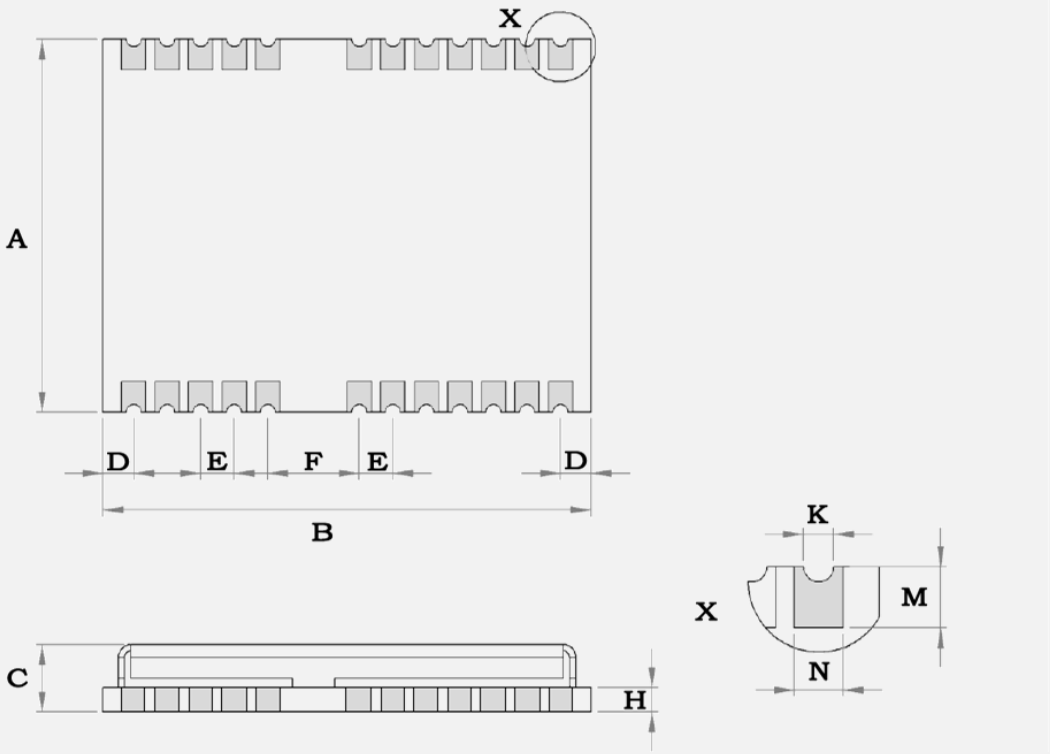


Figure 11 Dimensions

Table 11 Dimensions

Symbol	Min.(mm)	Typ.(mm)	Max.(mm)
A	12.0	12.2	12.4
B	15.8	16.0	16.2
C	2.2	2.4	2.6
D	0.9	1.0	1.3
E	1.0	1.1	1.2
F	2.9	3.0	3.1
H	--	0.8	--
K	0.4	0.5	0.6
M	0.8	0.9	1.0
N	0.7	0.8	0.9

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7 REFERENCE DESIGN

7.1 Reference Design

The RF_IN pin provides an active antenna with a power supply via the built-in inductor, therefore, the connection between the ANT_BIAS and RF_IN pins is no longer necessary, as shown in Figure 12.

If the active antenna requires a voltage or current that ANT_BIAS cannot provide, an external power supply shall be used and a DC blocking capacitor connected in series with RF_IN, as shown in Figure 13.

The characteristic impedance from the RF_IN pin to the antenna connector should be 50Ω

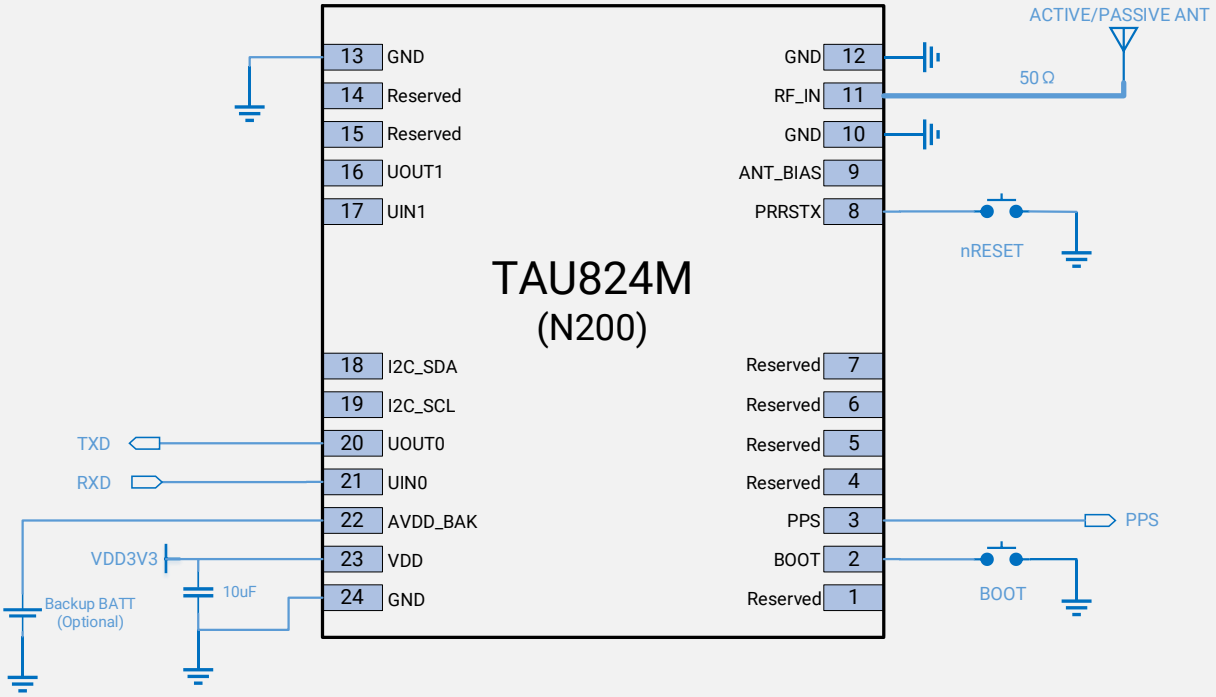


Figure 12 Reference design of active ant. supplied by ANT_BIAS

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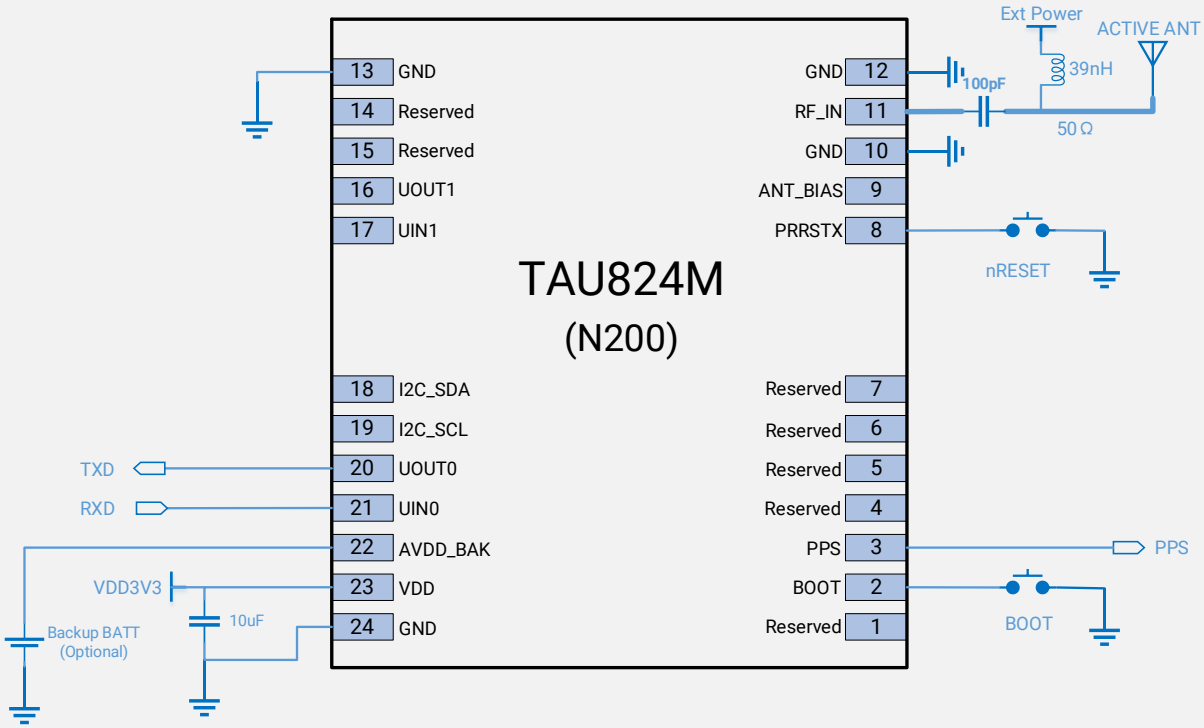


Figure 13 Reference design of active ant. supplied by external power

7.2 PCB Footprint Reference

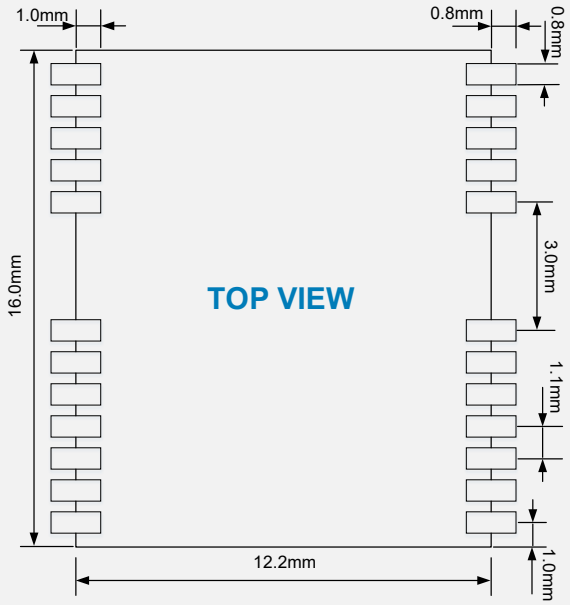


Figure 14 PCB Footprint Reference

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7.3 Layout Notes

1) A decoupling capacitor should be placed close to VDD pin of the module, and the width of power routing should be more than 0.5 mm.

2) The width of RF routing between RF port to antenna interface should be wider than 0.2 mm. The characteristic impedance of RF routing between RF port to antenna interface should be controlled to 50Ω.

3) It is recommended that the routing from RF port to antenna interface refers to the second layer, and no routing are recommended on the layer.

4) Do not place the module close to any EMI source, like antenna, RF routing, DC/DC or power conductor, clock signal or other high-frequency switching signal, etc.

5) When designing the PCB layout, it is important to position modules away from audio links to avoid interference with audio-related components.

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8 REFLOW SOLDERING

The heating or reflow phase will produce a liquid phase temperature exceeding 217°C–221°C. It is necessary to prevent a sudden increase in temperature. Otherwise, it will increase the risk of solder paste collapse.

- Liquid phase temperature above 220°C: 60s-90s
- Peak temperature: 235°C -245°C
- Soak time (170°C -220°C): 60s-120s
- Ramp-up slope: ≤3°C/s
- Ramp-down slope: -4°C/s to -1°C/s

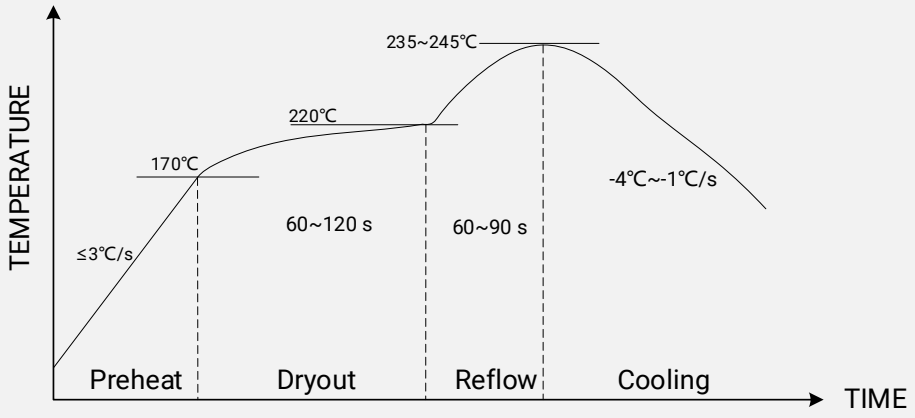


Figure 15 Recommended profile

The actual soldering temperature is influenced by external factors, such as the solder paste used, the size of the board, its thickness and design. If the actual peak temperature exceeds the recommended limit, there is a high risk of permanent damage to the module.

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9 PACKAGING INFORMATION

9.1 Packaging

The module is a Moisture Sensitive Device (MSD) and Electrostatic Sensitive Device (ESD). During packing and shipping, it is strictly required to take appropriate MSD handling instructions and precautions. The table below shows the general packing hierarchy for the standard shipment.

Table 12 Packing hierarchy

Module	Reel	Sealed bag	Packing box	Shipping carton
				

9.1.1 Tape and Reel

TAU824M-N200 is delivered as hermetically sealed, reeled tapes in order to enable efficient production, production lot set-up and tear-down. The figure below shows the tape dimensions.

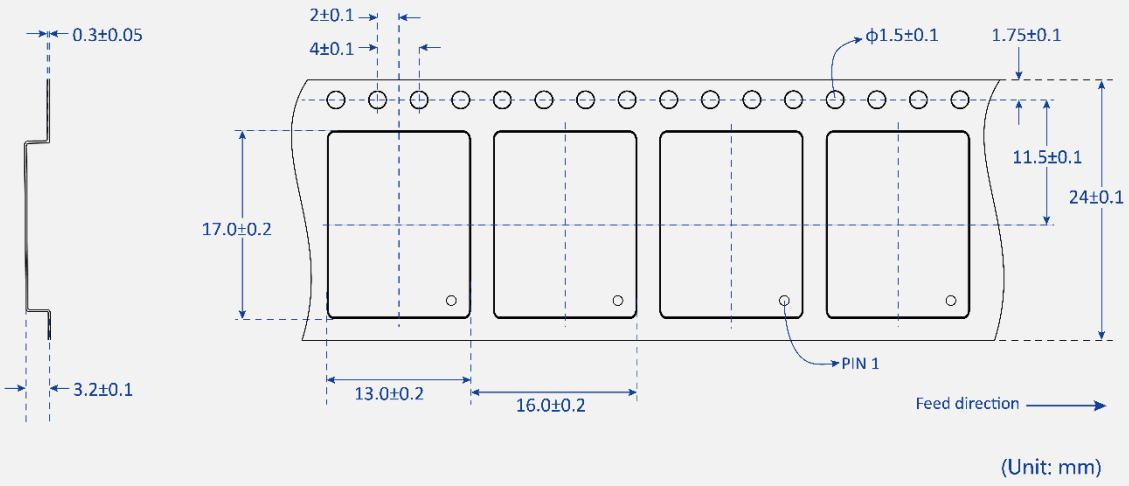


Figure 16 Tape dimensions

The module is deliverable in quantities of 1000 pcs on a reel. The figure below shows the dimensions of the reel.

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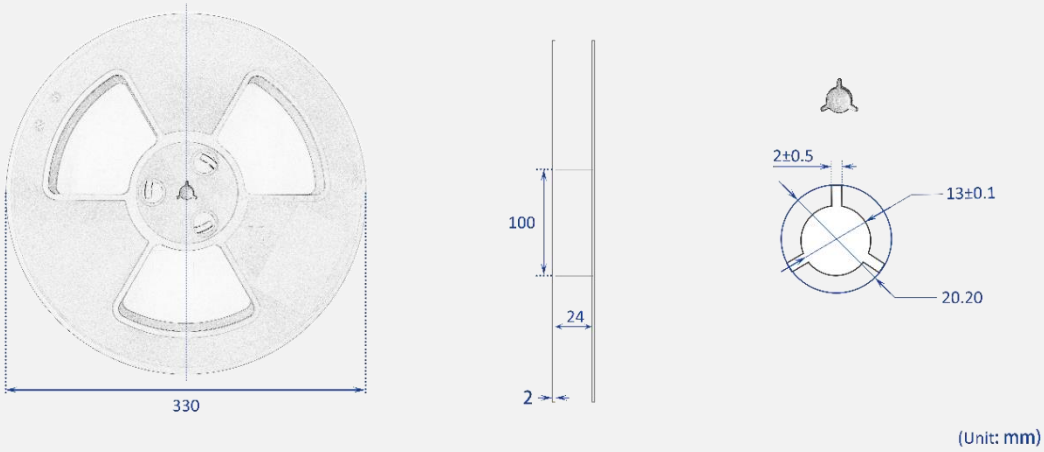


Figure 17 Reel dimensions

9.1.2 Shipment Packaging

The reels are packed in the sealed bags in a box and shipped by shipping cartons. Up to five boxes (1000 pcs in total) can be packed in one shipping carton.

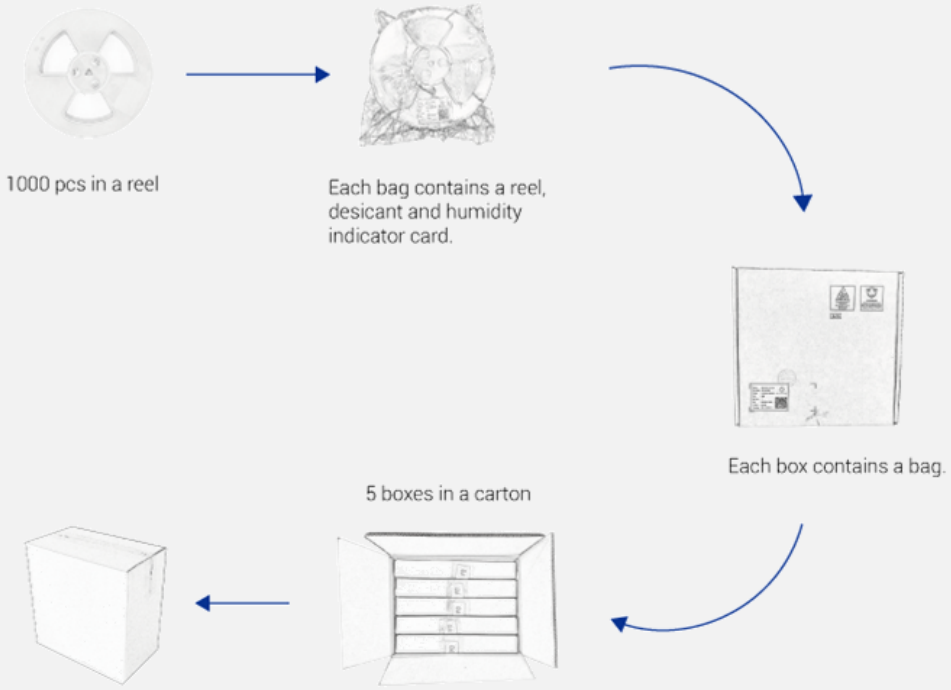


Figure 18 Packaging

9.2 Storage

In order to prevent moisture intake and protect against electrostatic discharge, the module is packaged together with a humidity indicator card and desiccant to absorb humidity.

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9.3 ESD Handling

9.3.1 ESD Handling Precautions

TAU824M-N200 which contains highly sensitive electronic circuitry is an Electrostatic Sensitive Device (ESD). Observe precautions for handling! Failure to observe these precautions may result in severe damage to the GNSS module!

- Unless there is a galvanic coupling between the local GND (i.e. the workbench) and the PCB GND, then the first point of contact when handling the PCB must always be between the local GND and PCB GND.
- Before mounting an antenna patch, connect ground of the device.
- When handling the RF pin, do not come into contact with any charged capacitors and be careful when contacting materials that can develop charges (e.g. patch antenna ~10 pF, coax cable ~50 - 80 pF/m, soldering iron …)
- To prevent electrostatic discharge through the RF input, do not touch any exposed antenna area. If there is any risk that such exposed antenna area is touched in non ESD protected work area, implement proper ESD protection measures in the design.
- When soldering RF connectors and patch antennas to the module's RF pin, make sure to use an ESD safe soldering iron (tip).



9.3.2 ESD Protection Measures

The GNSS positioning module is sensitive to static electricity. Whenever handling the module, particular care must be exercised to reduce the risk of electrostatic charges. In addition to standard ESD safety practices, the following measures should be taken into account.

- Add an ESD protective device to the RF input part to prevent electrostatics discharge.
- Do not touch any exposed antenna area.
- Add an ESD protective device to the UART interface.

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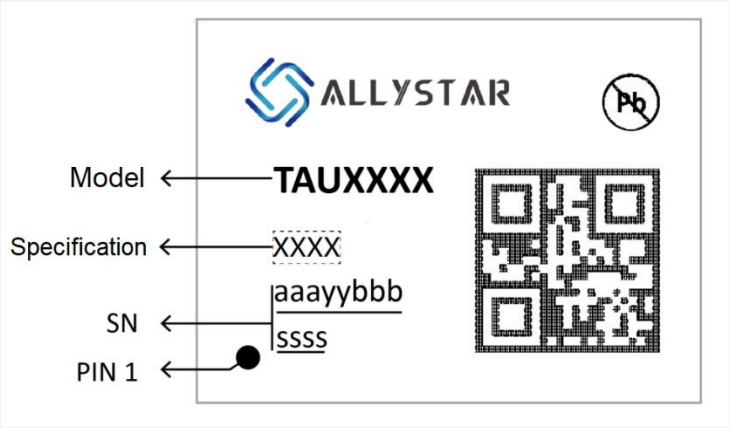
9.3.3 Moisture Sensitivity Level

The Moisture Sensitivity Level (MSL) of the GNSS module is MSL3.

10 LABELING AND ORDERING INFORMATION

Labeling and ordering information help customers get more about Allystar products.

10.1 Labeling



Symbol	Explanation	Sample
TAUXXXX	Product model for market promotion.	TAU824M
XXXX	Specification.	N200
aaayybbbssss	Serial number	392190010001

10.2 Ordering info

Table 13 Ordering codes

Ordering No.	Product info.
TAU824M-N200	Concurrent GNSS dual-band LCC Module, TCXO, Flash, LDO, 16×12.2 mm, 1000 pieces/reel

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11 RELATED DOCUMENTS

[1] Hardware Application Guide for GNSS Modules

[2] Satrack User Manual

[3] Allystar Common Commands

[4] GNSS Protocol Specification

12 REVISION HISTORY

Revision	Date	Revised by	Status/Comments
V1.0	2026-03	Berry	First release.

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